# N- and P-Channel 30-V (D-S) MOSFET

## CHARACTERISTICS

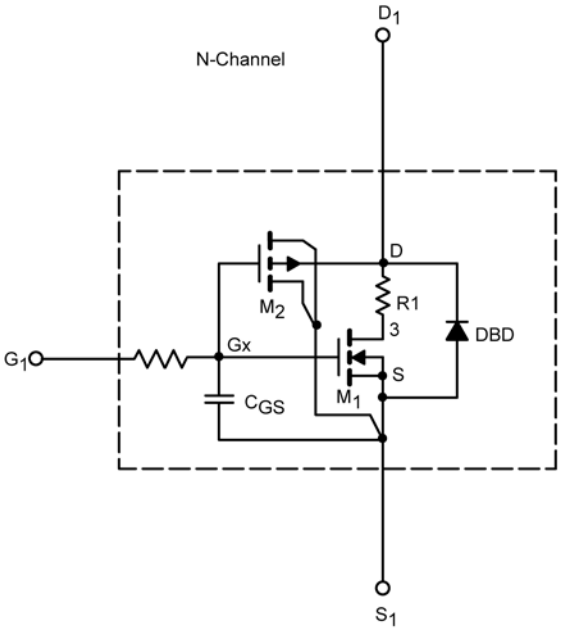
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

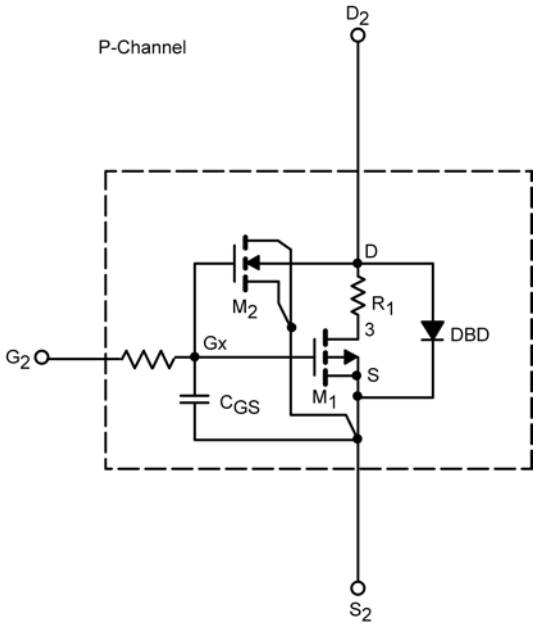
## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 4.5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC



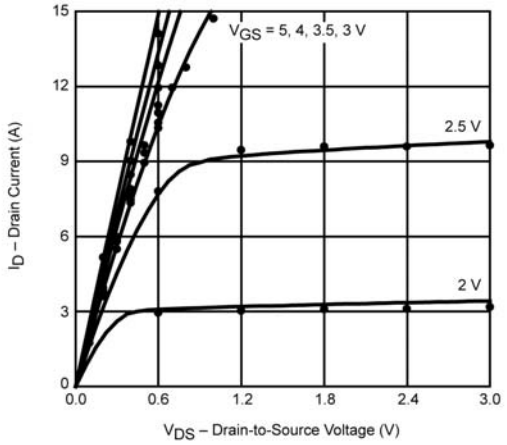

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

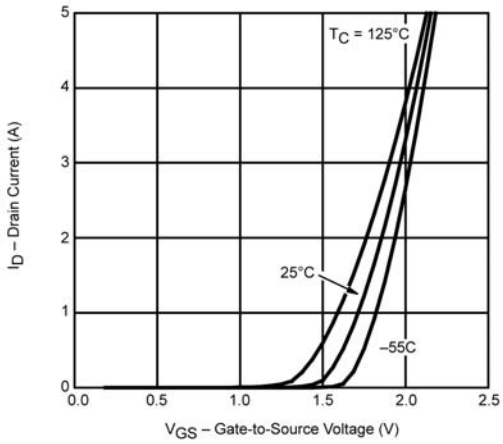
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N-Ch | 1.1 | | |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | P-Ch | 1.1 | | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ ≤ 5V, $V_{GS}$ = 4.5V | N-Ch | 54 | | A |
| | | $V_{DS}$ ≤ – 5V, $V_{GS}$ = – 4.5V | P-Ch | 27 | | |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 4.5V, $I_D$ = 4.8A | N-Ch | 0.041 | 0.045 | Ω |
| | | $V_{GS}$ = – 4.5V, $I_D$ = – 2.3A | P-Ch | 0.098 | 0.114 | |
| | | $V_{GS}$ = 2.5V, $I_D$ = 3.8A | N-Ch | 0.065 | 0.075 | |
| | | $V_{GS}$ = – 2.5V, $I_D$ = – 1.8A | P-Ch | 0.171 | 0.190 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15V, $I_D$ = 4.8A | N-Ch | 13 | 10.8 | S |
| | | $V_{DS}$ = – 15V, $I_D$ = – 2.3A | P-Ch | 6.7 | 6.56 | |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 2.4A, $V_{GS}$ = 0V | N-Ch | 0.73 | 0.80 | V |
| | | $I_S$ = – 1.5A, $V_{GS}$ = 0V | P-Ch | 0.80 | - 0.80 | |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | N-Channel $V_{DS}$ = 15V, $V_{GS}$ = 4.5V, $I_D$ = 4.8A; P-Channel $V_{DS}$ = – 15V, $V_{GS}$ = – 4.5V, $I_D$ = – 3.2A | N-Ch | 3.7 | 4.2 | nC |
| | | | P-Ch | 3.1 | 3.8 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | 1.1 | 1.1 | |
| | | | P-Ch | 0.60 | 0.60 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | 0.90 | 0.90 | |
| | | | P-Ch | 1.85 | 1.85 | |

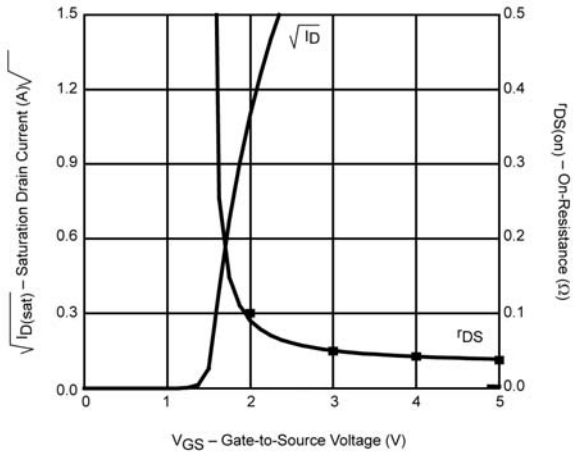
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
a. Guaranteed by design, not subject to production testing.

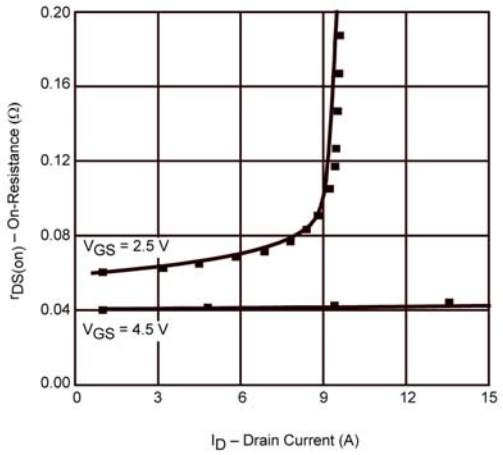
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

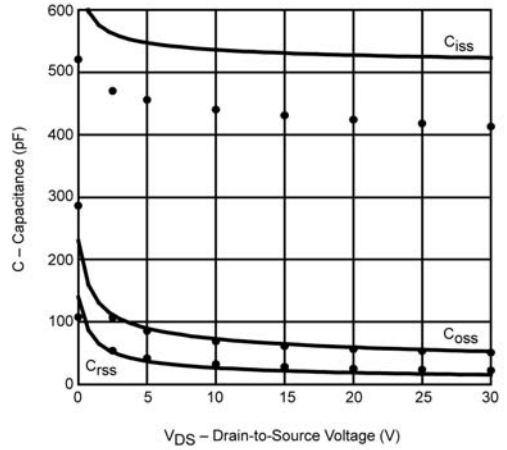
**N-Channel MOSFET**

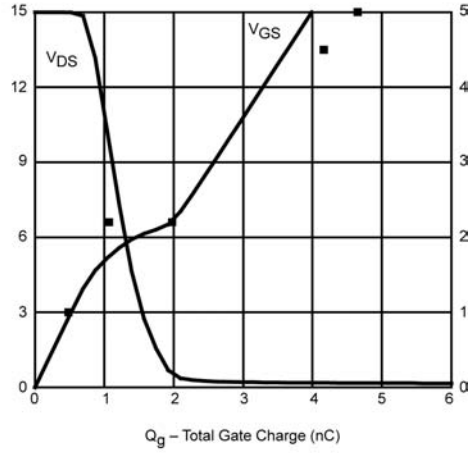


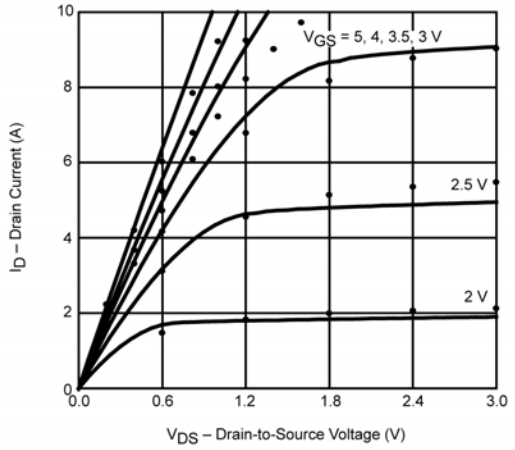



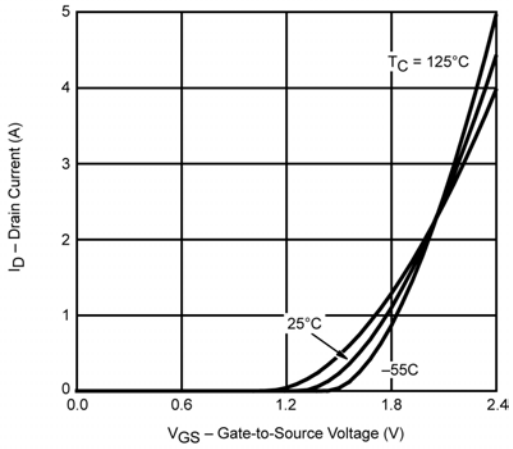



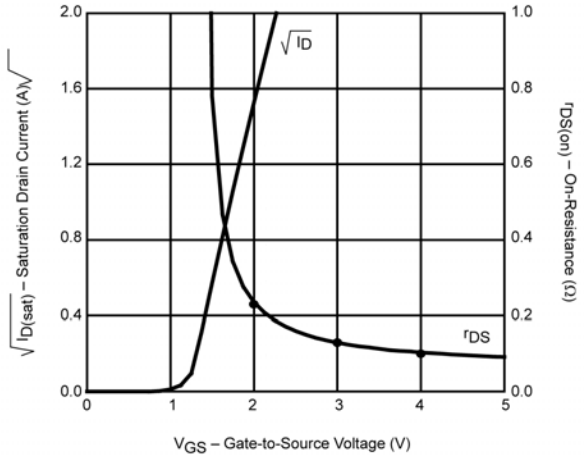



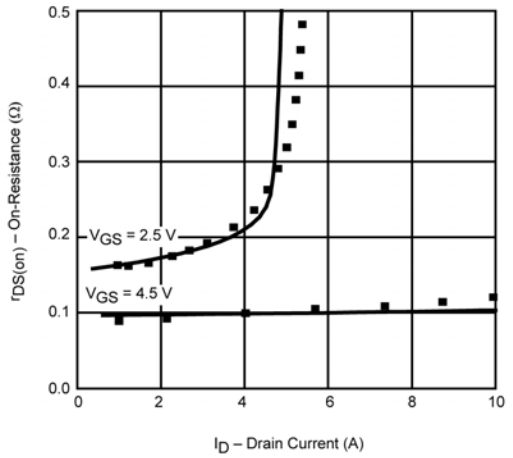

Note: Dots and squares represent measured data.

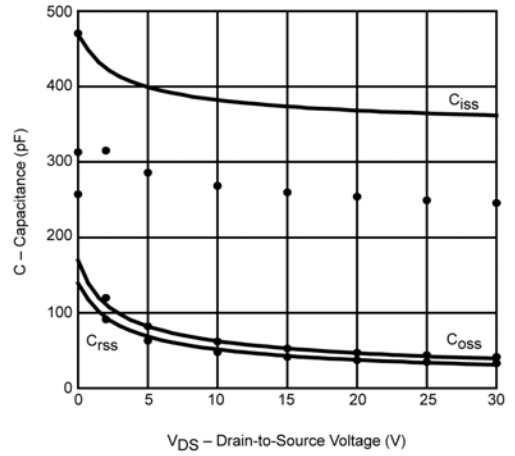
**P-Channel MOSFET**

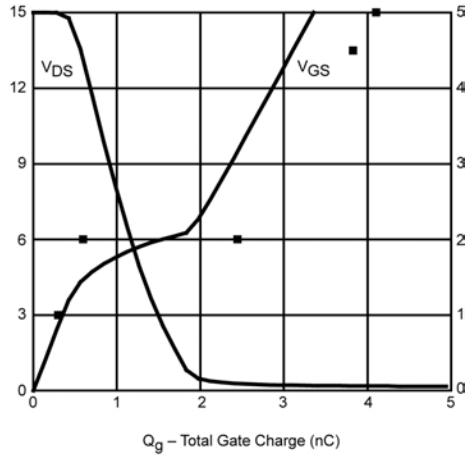



Note: Dots and squares represent measured data.

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